COMMUNICATION PORT CONTROL MODULE FOR LIGHTING SYSTEMS

TECHNICAL FIELD

The present invention relates to lighting control networks, and more particularly, to an improved communication port control module ("CPCM") that acts as a serial interface to a network control computer for a lighting system. The present invention also relates to a system that offloads much of the processing normally required of a microprocessor at the lighting device being controlled, instead performing such processing in hardware contained in an interface device interposed between the lighting device being controlled and the control computer controlling said lighting device.

BACKGROUND OF THE INVENTION

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~~Centralized lighting control systems are known in the art. Typically, the central computer~~ controls the lighting system throughout a building or other facility, such ~~as is~~ defined by the DALI standard, a well-known lighting control standard. ~~The~~ lighting device being controlled interfaces to the central computer ~~through~~ a serial interface. A microprocessor at the lighting device usually ~~performs~~ parallel to serial conversion of incoming commands and data, error ~~detection, and arbitration control between incoming and outgoing data and commands.~~ A1

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~~Figure 1 shows typical prior art interface into a DALI control computer. The control~~ computer 107 receives and transmits various data and commands ~~serially~~ over lines 103 and 104 as shown. A microprocessor 101 is employed at ~~the~~ lighting device to receive and process the commands and to control other ~~elements~~ of the lighting device over parallel bus 102. Functions executed by ~~microprocessor~~ 101 include error detection and correction, parallel to serial ~~conversion, and edge detection, as required by the DALI standard. Control of arbitration of~~

~~communications into and out of the lighting device is also implemented within microprocessor 101.~~ A2

One problem with prior art systems such as that of Figure 1 is that for cost reasons, microprocessor 101 is typically a basic low end capability processor such as an 8051. The tasks required to be performed by microprocessor 101 results in significant loading on the processor's limited capabilities, and decreased performance. The foregoing is true particularly with respect to error detection and correction algorithms, where significant mathematical processing may be required.

In view of the foregoing, there exists a need in the art for an improved technique of interfacing with a central lighting control computer that controls one or more lighting devices using a standard set of commands and a predetermined protocol.

There also exists a need in the art for an improved technique of minimizing the processing load presented to the basic capability microprocessors typically employed by a DALI compliant lighting device being controlled by a control computer.

SUMMARY OF THE INVENTION

The above and other problems of the prior art are overcome in accordance with the present invention, which relates to an improved method and apparatus for interfacing a central lighting control computer to a lighting device. In accordance with the invention, a separate hardware device is interposed between the microprocessor located at the lighting device, and the control computer controlling the device.

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~~The separate device is implemented in hardware to perform error detection, noise filtering, and optionally other functions previously performed by the microprocessor, such as parallel to serial conversion, serial to parallel conversion, edge detection, arbitration control, and possibly others. The hardware device interposed between the lighting device and the control~~

~~computer offloads much of the functionality from the microprocessor,~~ providing faster operating speeds and permitting better use of less expensive microprocessors typically employed at such lighting devices. In a preferred embodiment, the parallel to serial conversion is implemented as a preshift register ~~and a shift~~ register, and the error detection is implemented in common hardware ~~with parallel to serial conversion.~~ A3

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a prior art lighting device microprocessor interfacing to a control computer;

Figure 2 depicts a block diagram of an exemplary embodiment of the present invention, showing a hardware device interposed between the lighting device microprocessor and the network control computer; and

Figure 3 depicts a more detailed block diagram of an exemplary embodiment of a hardware device of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 depicts a block diagram of a hardware device CPCM 201 connected to a microprocessor 202. Not shown in Figure 2 is the lighting device controlled by microprocessor 202. Figure 2 includes a plurality of signals interfacing between CPCM 201 and microprocessor 202.

A decoder 219 and address lines 216 serve to permit communications to and from CPCM 201 over a parallel computer bus as is known in the art. More specifically, CPCM 201 is at a particular address known to microprocessor 202 and that address is asserted on the bus when communications with CPCM 201 are desired by the microprocessor. Several of the address lines are used for a chip select signal 218 and the remainder utilized as signal 216 in order to select the

appropriate location within CPCM 201. Typically the most significant bits are utilized to decode as a chip select signal, and any remaining bits of the address are used to identify a location within the CPCM.

Pro A4

~~Signals 214 and 215 represent the data bus exchanging data between microprocessor 202 and CPCM 201. Also in a conventional fashion, read and write signals 213 and 212, respectively, are utilized, and an interrupt signal 211 advises microprocessor 202 when the CPCM 201 wishes to transfer data. A reset signal and clock signal 221 are also used conventionally. Note that preferably clock signal 221 is the same clock signal utilized for both CPCM 201 and microprocessor 202 in order to synchronize the system.~~ A4

Serial interfaces 230 and 231, to and from the control computer respectively, serve to interface the lighting device to the control computer so that the control computer may be configured as in the prior art. More particularly, the control computer need not have any knowledge that the CPCM hardware device 201 has been interposed between the control computer and the lighting device microprocessor 202. Thus, the standard commands that control intensity, timing, etc., as set forth in the exemplary DALI standard described below herein, may be used. Such an arrangement permits the control computer to operate with the same software that it uses in conventional systems, not being concerned with the fact that a separate hardware device has been placed between the light being controlled and the control computer.

Preferably, the arrangement of Figure 2 implements the exemplary DALI standard interface, which provides for the exchange of commands and data on lines 230 and 231 in a serial fashion. The DALI interface is widely published and available and those who are skilled in the art are typically familiar with the standard.

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~~Figure 3 represents a more detailed hardware diagram to implement the functions of error detection, serial to parallel conversion, edge detection and arbitration control for signals entering~~

~~and exiting from the CPCM 201. The host interface 310 transmits and receives parallel data over a PC conventionally.~~ A5

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~~In operation, data is received serially from the control computer and entered into a~~ preshift register 301. The error detection noise filtering and ~~parallel~~ to serial conversion is implemented in conjunction with the pre-shift ~~and~~ shift registers 301 and 302, respectively. The error detection is a hardware circuit that detects particular bit patterns in the incoming data, ~~which violate rules of parity or other error detection techniques.~~ A6

An edge detection circuit 304 helps to further detect certain errors. More specifically, in the exemplary embodiment utilizing the DALI Standard, each bit must have an edge since the data is encoded in a manner that a change of state takes place within each bit. Logical ones have a state transition in a first direction, and logical zeroes in a second direction. The failure to detect such an edge represents an error which should be detected by edge detect circuit 304. A straight forward arrangement of logic circuitry can detect the absence of such an edge, or latch its presence, to ascertain whether an error has occurred.

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~~Additionally, the start of data is noted in the DALI Standard by a falling edge which is~~ also detected by an edge detect circuit 304, and conveyed to an arbitration ~~control~~ logic 306. The arbitration control logic 306 ensures that data being held in locations 321 through 327 is not overwritten by new data before it is read out ~~by the~~ microprocessor. Conventional logic may be used to implement such a system wherein no new data is rewritten into any register 321 through 327 until the previous data is read out. A clock divider 340 serves to operate the CPCM at a rate ~~sufficient to allow for the parallel to serial conversion.~~ A7

Ins A8

~~Registers 321 through 327 are special function registers. Register 321 is the clocking~~ register and is used to set or adjust the data rate ~~in order~~ to provide for signals being read and ~~written to and from the microprocessor and the control computer at different rates. More~~

~~specifically, the parallel to serial conversion requires that the serial interface operate at many times the speed of the parallel interface in order to keep up with data being sent in parallel.~~ A8

Register 322-324 stores DALI known commands such as address signals, standard data and other DALI commands. These commands and data would normally be stored in the microprocessor memory in prior systems, where no hardware CPCM is interposed between the control computer and the lighting device. The MOP register 325 is used to store a value indicative of manual dimming, in the event the manual dimming override is utilized to control the lighting device manually rather than via the control computer. Diagnostic computer 327 stores error codes and operating states in order to diagnose problems in a conventional fashion.

A9 ~~In operation, serial data arrives by via line 351 and is shifted into preshift register 301.~~ The data is not shifted into register 302 until it has been verified as correct via the error detection and P/S control block 303. Since the preshift register 301 is typically smaller that the shift register 302, the data from the preshift register 301 will be shifted to the shift register 302 plural times for each readout from the shift register 302. The error detection is performed in the smaller preshift register 301, and the data is only shifted to shift register 302 after passing the error detection testing in preshift register 301. Hardware device 303 is an error detection system which will substantially immediately detect signaling errors should such an error occur. The generation of such an error will be signaled back to the control computer, and the DALI protocol ~~provides for the retransmission of such erroneously transmitted signals.~~ A9

Additionally, if edge detector 304 detects a violation of the DALI protocol, such an error will also be conveyed to the microprocessor. In the exemplary DALI protocol, for example, a falling edge followed by a predetermined length "low" signal is required to being transmission of data, and an edge is required during each bit time. A violation of this rule indicates an error.

Note from interface 310 that only parallel data is transmitted to and from the microprocessor interface, and that such parallel data has already been checked for errors, and

protocol violations, and is ready for decoding. Accordingly, the microprocessor at the lighting device may perform nothing more than the decoding of DALI commands and data. Such a system provides that the software in the microprocessor only perform a table lookup and basic control functions and does not require any error correction algorithms or arbitration control. This greatly increases speed.

While the above describes the preferred embodiment of the invention, various other modifications and additions will be apparent to those of skill in the art. Such modifications and additions are intended by the following claims.